# *SERVICE MANUAL*

# 1581
# 3.5 DISK DRIVE

**JUNE 1987** **PN-314982-01**

**Commodore Business Machines, Inc.**
1200 Wilson Drive, West Chester, Pennsylvania 19380 U.S.A.

# TABLE OF CONTENTS

# GENERAL SPECIFICATIONS

## 1 CHARACTERISTICS

A) 3.5 inch, +800K storage
B) Increased buffers, fixed BAM locations
C) Expanded controller commands
D) Track cache buffer
E) Configurable auto boot file
F) User alterable physical/logical track and sector translation
G) Fully vectored jump table
H) Partition capabilities
I) Wild card enhancements
J) Standard, fast and burst serial capabilities
K) Expanded burst command set

## 2 HARDWARE SUMMARY

*PROCESSORS:* 6502A, WD1770
*ROM:* 32K
*RAM:* 8K
*I/O:* 8520A

## 3 SPECIFICATIONS

*GROSS DATA ORGANIZATION:*

3.5 Inch Disk
Double-Sided
80 Cylinders/160 Tracks

*PER TRACK ORGANIZATION:*

Hex 4E written as a gap, with 10 sectors of data, with full gaps written for motor speed variation.

*PER SECTOR ORGANIZATION:*

MFM Encoding
12 Bytes of 00
3 Bytes of Hex A1 (Data Hex A1, Clock Hex 0A)
1 Byte of FE (ID Address Mark)
1 Byte (Track Number)
1 Byte (Side Number)
1 Byte (Sector Number)
1 Byte (Sector Length, 02 for 512 Byte Sectors)
2 Bytes CRC (Cyclic Redundancy Check)
22 Bytes of Hex 22

## 3 SPECIFICATIONS *(continued)*

12 Bytes of 00
3 Bytes of Hex A1 (Data Hex A1, Clock Hex 0A)
1 Byte of Hex FB (Data Address Mark)
512 Bytes of Data
2 Bytes of CRC (Cyclic Redundancy Check)
38 Bytes of Hex 4E

## 4 FORMAT ORGANIZATION

*PHYSICAL:*

Cylinders 0 thru 79
Sectors 1 thru 10 on Side 1
Sectors 1 thru 10 on Side 2
Sector Size 512

*LOGICAL:*

Tracks 1 thru 80
Sectors 0 thru 39 (Using physical Sectors 1...10 — Side 1 and 2)
Sector Size 256 Bytes

*STORAGE:*

| | |
|---|---|
| Total Unformatted Capacity | 1 Megabyte |
| Total Formatted Capacity | 808, 960 Bytes |
| Maximum Sequential File Size | 802, 640 Bytes |
| Maximum Relative File Size | 182, 880 Bytes |
| Records Per File | 65, 535 |
| Files Per Diskette | *296 |
| Cylinders Per Diskette | 80 |
| Logical Sectors Per Cylinder | 40 |
| Physical Sectors Per Cylinder | 20 |
| Logical Bytes Per Sector | 256 |
| Physical Bytes Per Sector | 512 |
| Free Blocks Per Disk | 3160 |

*More with Sub-Disk Partitioning

## 5 MEMORY MAP — I/O LOCATIONS

| | | |
|---|---|---|
| 8K x 8 RAM | $0002-$1FFF | |
| 8520A | $4000-$4010 | Controller, Serial Bus |
| WD 1770 | $6000-$6003 | MFM Disk Controller |
| 32K x 8 ROM | $8000-$FFFF | DOS, Controller Code |

## 6 MEMORY MAP — RAM USAGE

| | |
|---|---|
| $0002-$00FF | Zero Page Variables |
| $0100-$01FF | Vectors, Variables and Stack Area |
| $0200-$02FF | Command/Error Buffer and Variables |
| $0300-$03FF | Buffer #0 |
| $0400-$04FF | Buffer #1 |
| $0500-$05FF | Buffer #2 |
| $0600-$06FF | Buffer #3 |
| $0700-$07FF | Buffer #4 |
| $0800-$08FF | Buffer #5 |
| $0900-$09FF | Buffer #6 |
| $0A00-$0AFF | BAM |
| $0B00-$0BFF | BAM |
| $0C00-$1FFF | Track Cache Buffer |

## 7 COMMODORE SERIAL INTERFACE

The 1581 supports Standard, Fast, and Fast Serial communication like the 1571.

A HRF (Host Request Fast) command places the drive in fast serial mode. The 1581 remains in fast serial mode until an Unlisten, Untalk, or serial bus error. The 1581 will also source a DRF (Device Request Fast) message. This message lets the host know that the addressed peripheral can receive bytes fast (or slow).

The bus consists of the following:

*PIN 1 — SRQ (Service Request)*

Unused by the current serial bus. Fast serial will use this line as a bi-direction fast clock line.

*PIN 2 — GND*

Chassis ground.

*PIN 3 — ATN (in)*

The host brings this signal low which then generates an interrupt on the controller board. The attention sequence is followed by an address. If the device does not respond within a preset time, the host will assume the device addressed is not on the bus.

*PIN 4 — CLK (in/out)*

This signal is used for timing the data sent on the serial bus (software clocked).

*PIN 5 — DATA (in/out)*

Data on the serial bus is transmitted one bit at a time (software toggled). In addition, this line is wire 'ored' and used as a FAST DATA line to compliment the FAST CLOCK on the SRQ line.

*PIN 6 — RESET*

This line will reset the peripheral upon host reset.

## 8 PROGRAMMABLE BAUD RATE GENERATOR

The 8520 contains a programmable baud rate generator which is used for fast serial transfers. Timer A is used for the baud rate generator. In the output mode data is shifted out on SP at 1/2 the underflow rate of Timer A. The maximum baud rate possible is phi 2 divided by 4, but the maximum usable baud rate will be determined by line loading and the speed at which the receiver responds to the input data. Transmission will start following a write to the Serial Data Register (provided Timer A is running and in continuous mode). The clock derived from Timer A appears on the CNT pin. The Data in the Serial Data Register will be loaded into the shift register then shifted out to the SP pin. After 8 pulses on the CNT pin, a bit in the ICR (interrupt control register) is set and if desired, an interrupt may be generated. All incoming fast bytes generate an interrupt within the Fast Serial Drive. Bytes are shifted out; most significant bit first.

***NOTE:*** When the 8520 is put in output mode the SP pin (data) will go low.

| Baud Rate<br>Phi2 = 2MHz | Hi Timer Value | Low Timer Value |
|---|---|---|
| 166k | 00 | 06 |
| 143k | 00 | 07 |
| 100k | 00 | 10 |
| 50k | 00 | 20 |
| 25k | 00 | 40 |
| 12.5k | 00 | 80 |

## 9 SELF TEST DIAGNOSTICS

The 1581 performs a self-test of RAM, ROM, and Controller. If an error is detected, the DOS will blink all LED's a specific number of times. The flash code is repeated continuously.

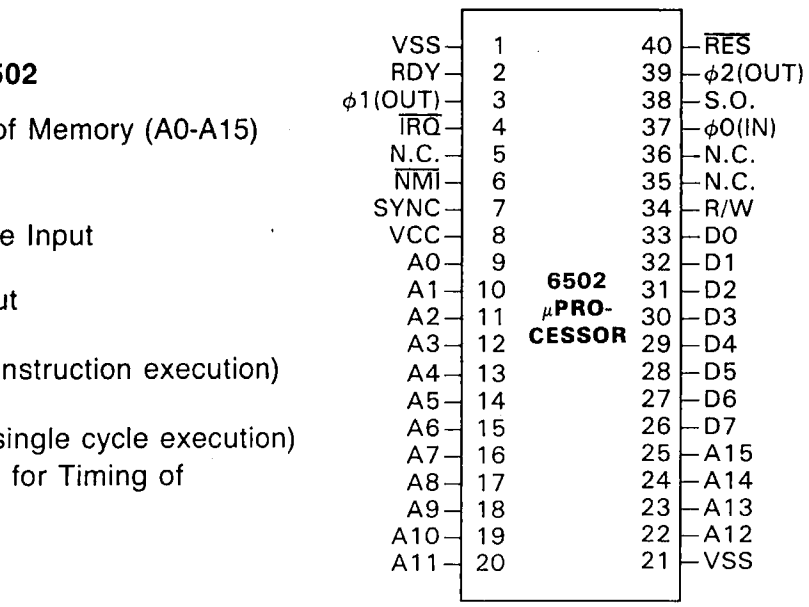
| # OF FLASHES | RESOURCE | COMPONENT |
|---|---|---|
| 1 | Zero Page | 8K x 8 RAM |
| 2 | ROM | 25256 |
| 3 | 100H-1FFFH | 8K x 8 RAM |

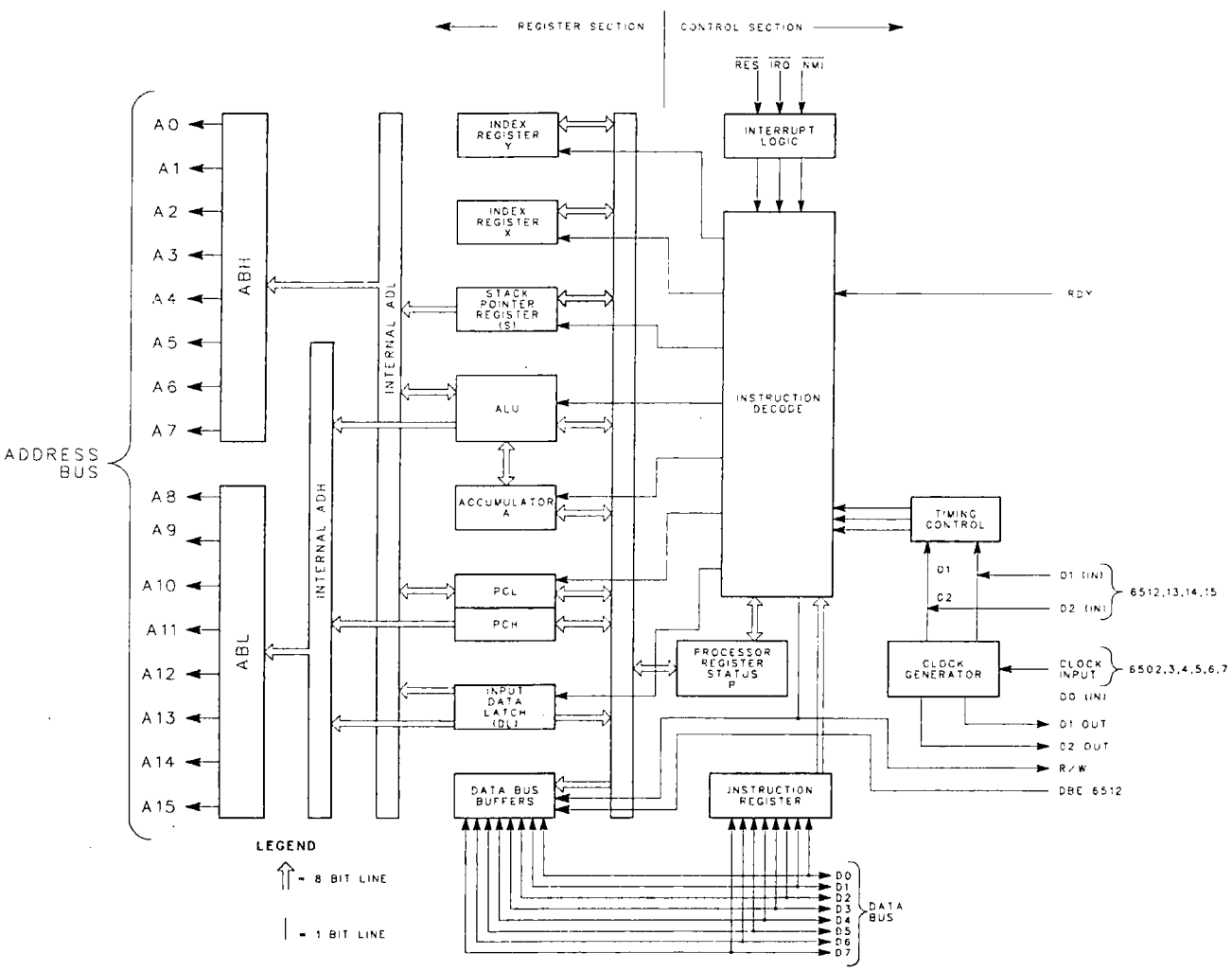
In addition, the 1581 performs a Controller Test. If a failure is detected, the error channel will contain 76, controller error 00,00. If an extensive test of ROM is required, the 1581 provides a signature analysis via command 'UO>T'. If a failure is detected, the LED's will blink 4 times continuously.

# 6502 MICROPROCESSOR

### Features of 6502

- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- On-the-chip Clock
  - TTL Level Single Phase Input
  - RC Time Base Input
  - Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two-Phase Output Clock for Timing of Support Chips
- $\overline{NMI}$ Interrupt



# 6502 SIGNAL DESCRIPTION

***Clocks ($0_1$, $0_2$)*** — The 651X requires a two phase non-overlapping clock that runs at the Vcc voltage level. The 650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

***Address Bus ($A_0$-$A_{15}$)*** — These outputs are TTL compatible, capable of driving one standard TTL load and 130 pf.

***Data Bus ($D_0$-$D_7$)*** — Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pf.

***Data Bus Enable (DBE)*** — This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation, DBE would be driven by the phase two ($0_2$) clock, thus allowing data output from microprocessor only during $0_2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

***Ready (RDY)*** — This input signal allows the user to single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during, or coincident with, phase one ($0_1$) and up to 100ns after phase two ($0_2$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($0_2$) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If Ready is low during a write cycle, it is ignored until the following read operation.

***Interrupt Request ($\overline{IRQ}$)*** — This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore, transferring program control to the memory vector located at these addresses. The RDY signal must be in high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

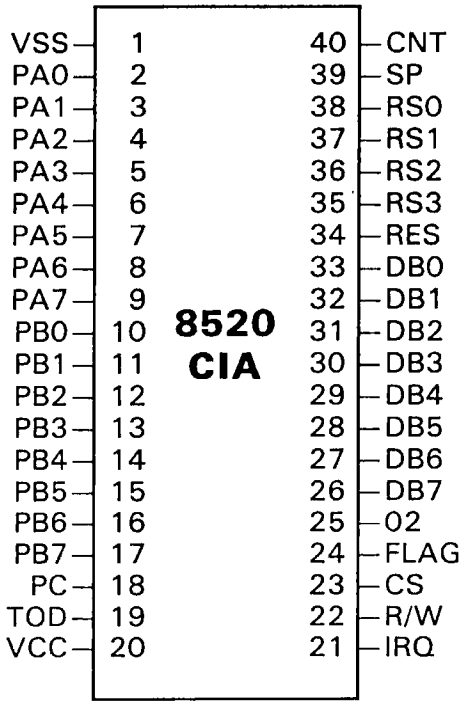
***Non-Maskable Interrupt ($\overline{NMI}$)*** — A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. $\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the interrupt mask flag status. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory. $\overline{NMI}$ also requires an external 3KΩ resistor to Vcc for proper wire-OR operations. Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are sampled during $0_2$ (phase 2) and will begin the appropriate interrupt routine on the $0_1$ (phase 1) following the completion of the current instruction.

***Set Overflow Flag (S.O.)*** — A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of $0_1$.

***SYNC*** — This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $0_1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $0_1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

***Reset*** — This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence. After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control. After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid. When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

# 8520A COMPLEX INTERFACE ADAPTER




## INTERFACE SIGNALS

***02 Clock Input*** — The 02 clock is a TTL, compatible input used for internal device operation and as a timing reference for communicating with the system data bus.

***CS — Chip Select Input*** — The CS input controls the activity of the 8520. A low level on CS while 02 is high causes the device to respond to signals on the R/W and address (RS) lines. A high on CS prevents these lines from controlling the 8520. The CS line is normally activated (low) at 02 by the appropriate address combination.

***R/W — Read/Write Input*** — The R/W signal is normally supplied by the microprocessor and controls the direction of data transfers of the 8520. A high on R/W indicates a read (data transfer out of the 8520), while a low indicates a write (data transfer into the 8520).

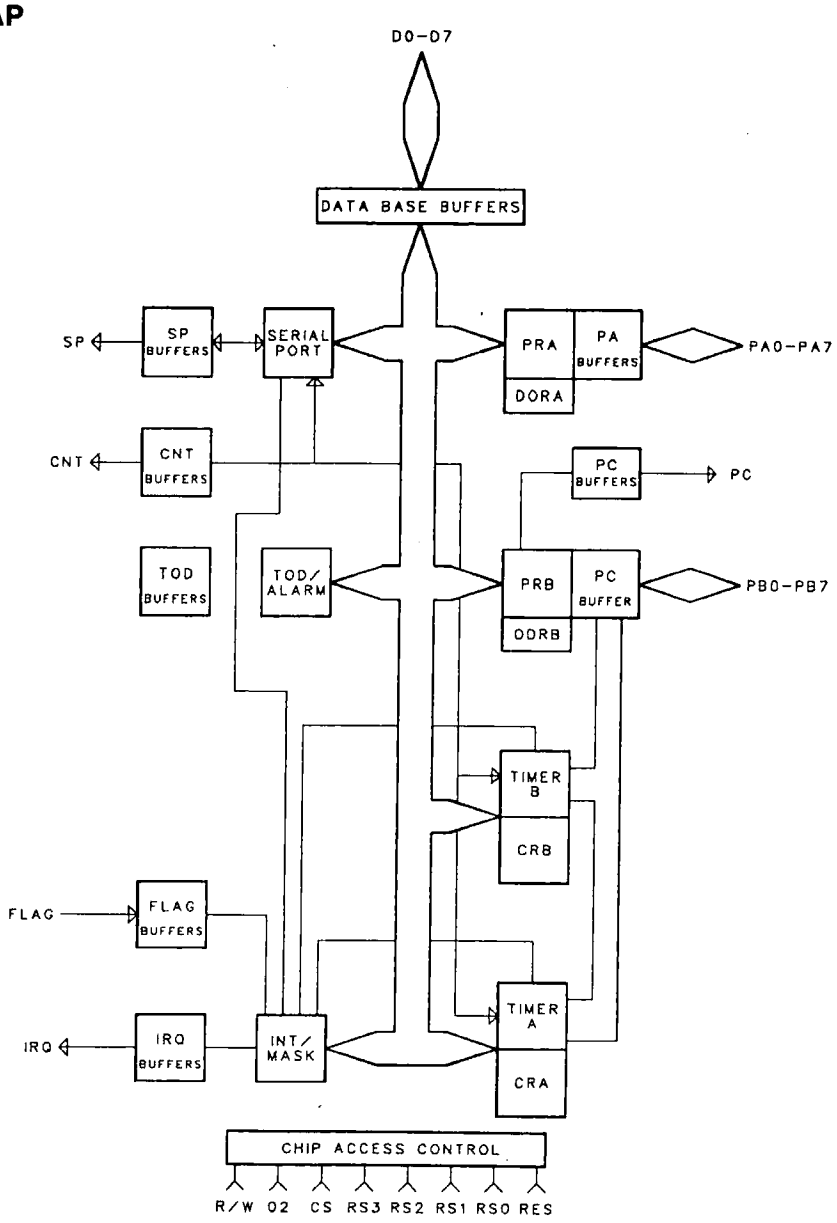
***RS3-RS0 — Address Inputs*** — The address inputs select the internal registers as described by the Register Map.

***DB7-DB0 — Data Bus Inputs/Outputs*** — The eight bit data bus transfers information between the 8520 and the system data bus. These pins are high impedance inputs unless CS is low and R/W and 02 are high, to read the device. During this read, the data bus output buffers are enabled, driving the data from the selected register onto the system data bus.

***IRQ — Interrupt Request Output*** — IRQ is an open drain output normally connected to the processor interrupt input. An external pullup resistor holds the signal high, allowing multiple IRQ-outputs to be connected together. The IRQ output is normally off (high impedance) and is activated low as indicated in the functional description.

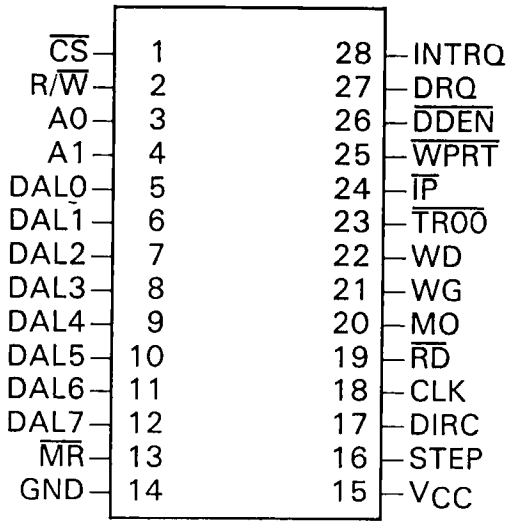
***RES — Reset Input*** — A low on the RES pin resets all internal registers. The port pins are set as inputs and port registers to zero (although a read of the ports will return all highs because of passive pullups). The timer control registers are set to zero and the timer latches to all ones. All other registers are reset to zero.

## REGISTER MAP



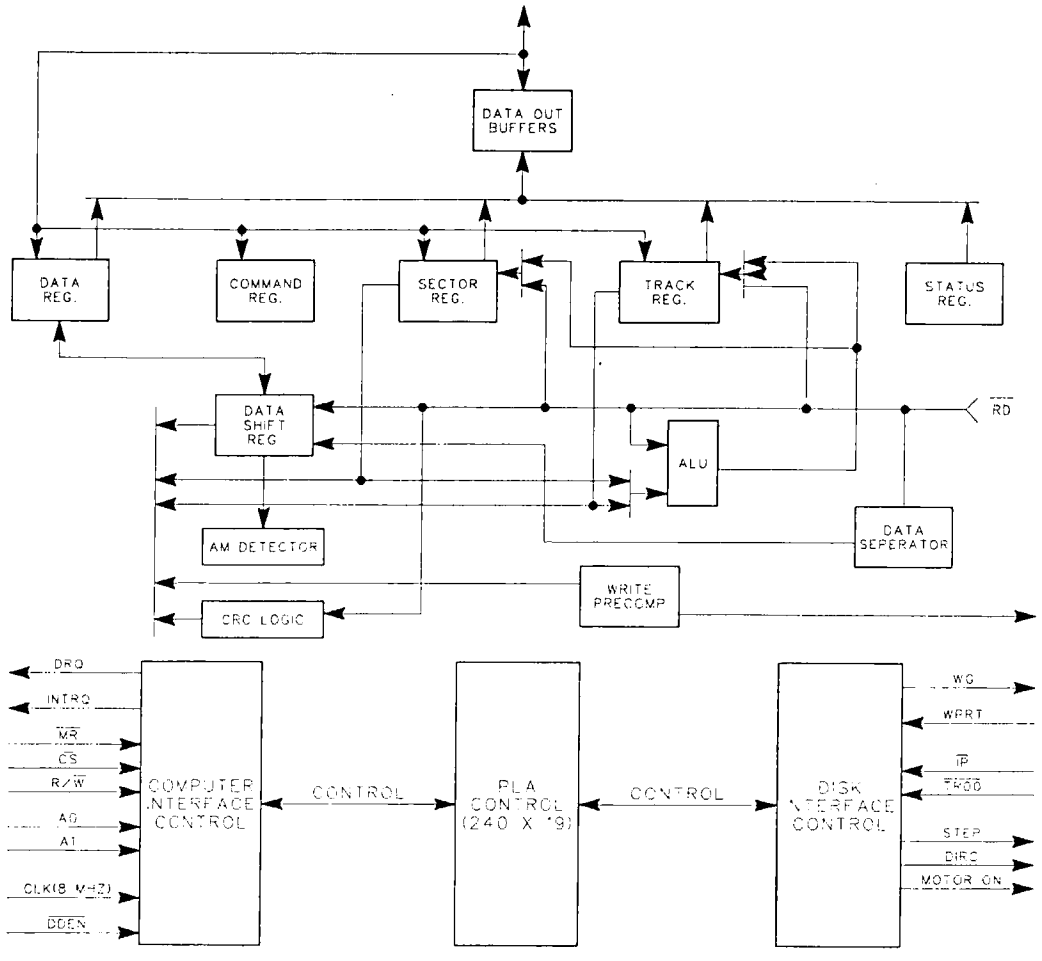

| RS3 | RS2 | RS1 | RS0 | REG | | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | PRA | Peripheral Data Reg. A |
| 0 | 0 | 0 | 1 | 1 | PRB | Peripheral Data Reg. B |
| 0 | 0 | 1 | 0 | 2 | DDRA | Data Direction Reg. A |
| 0 | 0 | 1 | 1 | 3 | DDRB | Data Direction Reg. B |
| 0 | 1 | 0 | 0 | 4 | TA LO | Timer A Low Register |
| 0 | 1 | 0 | 1 | 5 | TA HI | Timer A High Register |
| 0 | 1 | 1 | 0 | 6 | TB LO | Timer B Low Register |
| 0 | 1 | 1 | 1 | 7 | TB HI | Timer B High Register |
| 1 | 0 | 0 | 0 | 8 | | Event LSB |
| 1 | 0 | 0 | 1 | 9 | | Event 8-15 |
| 1 | 0 | 1 | 0 | A | | Event MSB |
| 1 | 0 | 1 | 1 | B | | No Connect |
| 1 | 1 | 0 | 0 | C | SDR | Serial Data Register |
| 1 | 1 | 0 | 1 | D | ICR | Interrupt Control Register |
| 1 | 1 | 1 | 0 | E | CRA | Control Register A |
| 1 | 1 | 1 | 1 | F | CRB | Control Register B |

# WD1770 FLOPPY DISK CONTROLLER




| | | | |
|---|---|---|---|
| 1 | CS | CHIP SELECT | A logic low on this input selects the chip and enable Host communication with the device. |
| 2 | R/W | READ/WRITE | A logic high on this input controls the placement of data on the D0-D7 lines from a selected register, while a logic low causes a write operation to a selected register. |
| 3,4 | A0,A1 | ADDRESS 0,1 | These two inputs select a register to Read/Write data: |
| 5-12 | DAL0-DAL7 | DATA ACCESS LINES 0 THRU 7 | Eight bit bidirectional bus used for transfer of data, control, or status. This bus is enabled by CS and R/W. Each line will drive one TTL load. |
| 13 | MR | MASTER RESET | A logic low pulse on this line resets the device and initializes the status register (internal pull-up). |
| 14 | GND | GROUND | Ground. |
| 15 | $V_{CC}$ | POWER SUPPLY | +5V ±5% power supply input. |
| 16 | STEP | STEP | The Step output contains a pulse for each step of the drive's RW head. The WD1770 and WD1772 offer different step rates. |
| 17 | DIRC | DIRECTION | The Direction output is high when stepping in towards the center of the diskette, and low when stepping out. |
| 18 | CLK | CLOCK | This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHZ ±1%. |
| 19 | RD | READ DATA | This active low input is the raw data line containing both clock and data pulses from the drive. |
| 20 | MO | MOTOR ON | Active high output used to enable the spindle motor prior to read, write or stepping operations. |
| 21 | WG | WRITE GATE | This output is made valid prior to writing on the diskette. |
| 22 | WD | WRITE DATA | FM or MFM clock and data pulses are placed on this line to be written on the diskette. |
| 23 | TR00 | TRACK00 | This active low input informs the WD1770 that the drive's R/W heads are positioned over Track zero (internal pull-up). |
| 24 | IP | INDEX PULSE | This active low input informs the WD1770 when the physical index hole has been encountered on the diskette (internal pull-up). |
| 25 | WPRT | WRITE PROTECT | This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing (internal pull-up). |
| 26 | DDEN | DOUBLE DENSITY ENABLE | This input pin selects either single (FM) or double (MFM) density. When DDEN = 0, double density is selected (internal pull-up). |
| 27 | DRQ | DATA REQUEST | This Active high output indicates that the data register is full (on a READ) or empty (on a Write operation). |
| 28 | INTRQ | INTERRUPT REQUEST | This Active high output is set at the completion of any command or reset or read of the status register. |

| CS | A1 | A0 | R/W = 1 | R/W = 0 |
|---|---|---|---|---|
| 0 | 0 | 0 | Status Reg | Command Reg |
| 0 | 0 | 1 | Track Reg | Track Reg |
| 0 | 1 | 0 | Sector Reg | Sector Reg |
| 0 | 1 | 1 | Data Reg | Data Reg |




## ARCHITECTURE

The Floppy Disk Formatter block diagram is illustrated on page 11. The primary sections include the parallel processor interface and the Floppy Disk Interface.

***Data Shift Register*** — This 8-bit register assembles serial data from the Read Data input ($\overline{RD}$) during Read operations and transfers serial data to the Write Data output during Write operations.

***Data Register*** — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired Track,position. This register is loaded from the DAL and gated onto the DAL under processor control.

***Track Register*** — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

***Sector Register (SR)*** — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

***Command Register (CR)*** — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

***Status Register (STR)*** — This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

***CRC Logic*** — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is:

$G(x) = x^{16} + x^{12} + x^5 + 1.$

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

***Arithmetic/Logic Unit (ALU)*** — The ALU is a serial comparator, incrementor, and decrementor, and is used for register modification and comparisons with the disk recorded ID field.

***Timing and Control*** — All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock. The FD1770 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0, double density (MFM) is enabled. When $\overline{DDEN}$ = 1, single density is enabled.

***AM Detector*** — The address mark detector detects ID, data and index address marks during read and write operations.

***Data Separator*** — A digital data separator, consisting of a ring shift register and data window detection logic, provides read data and a recovery clock to the AM detector.

## PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the WD1770. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and R/$\overline{W}$ = 1 are active or act as imput receivers when $\overline{CS}$ and R/$\overline{W}$ = 0 are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signal R/$\overline{W}$, during a Read operation or Write operation are interpreted as selecting the following registers:

| A1 - A0 | Read (R/$\overline{W}$= 1) | WRITE (R/$\overline{W}$= 0) |
|---|---|---|
| 0 0 | Status Register | Command Register |
| 0 1 | Track Register | Track Register |
| 1 0 | Sector Register | Sector Register |
| 1 1 | Data Register | Data Register |

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD1770 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations, the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations, the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data is set in the Status Register.

At the completion of every command, an INTRQ is generated. INTRQ is reset by either reading the status register, or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The WD1770 has two modes of operation according to the state $\overline{DDEN}$ (Pin 26). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 18) is at 8 MHZ.